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Implementation of PPM Modulation and Demodulation using NI Digital Electronics FPGA Board

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***Abstract* – In the paper, the use of NI LabVIEW FPGA module and NI Digital Electronics FPGA Board for the implementation of pulse position modulator and demodulator are considered. Different features of this development board was described. The measurements and tests of the system were carried out.**

Index terms – NI Digital Electronics FPGA Board, NI FPGA Module, Pulse-Position Modulation.

I. Introduction

In today's world, where reality is more and more replaced by virtual models, the development of individual nodes, and sometimes entire systems become more and more easy. FPGAs are often used in such projects. The complexity of using FPGAs is the need for programming skills in complex specific languages (VHDL, Verilog, etc). This stops engineers from using FPGAs in measurement and data acquisition applications. However, the combination of features and technology of Labview reconfigurable FPGA I/O allows us to consider the process of creating a virtual application from a different perspective. The use of FPGAs in the designing of hardware structure of control and measurement systems become less complicated with the help of Labview FGPA module [1].

In recent years, the feature of telemetry systems is a large number of various measured physical quantities and high accuracy. The design of such systems need expensive equipment and highly qualified personnel. Solutions proposed by NI can be applied to develop a downhole telemetry system with a radio channel and pulse position modulation [2–3].

II. Hardware and Software

NI Digital Electronics FPGA Board was used for the development of this project. It is an electronic circuits development tool built on the basis of FPGA XC3S500E Xilinx Spartan-3E. The board has a sufficient set of an additional controls and indicators. There are eight slide switches, four tactile buttons, two-digit seven-segment indicator, eight LEDs and push-rotary knob to select an external clock, etc. [4].

To work with the evaluation board you must have the following:

- NI Digital Electronics FPGA Board drivers
- NI LabVIEW 8.6 or higher, LabVIEW FPGA module
- Xilinx ISE WebPACK
- NI ELVIS II workstation with NI ELVISmx 4.0 software

The necessary components have been installed in accordance with installation instructions.

The transmitting side of the system was assembled to work in the NI ELVIS mode, and the receiving side to work offline. NI ELVIS II+ laboratory station opportunities was used for measurements and debugging. In particular, we used the following Vis. In particular:

- Variable Power Supply enables output voltage in the range of -12 to +12 volts. The signal from the source is sent to the 1:4 voltage divider, and the output of the divider is connected to analog-to-digital convertor.

Supply. This signal is connected to a voltage divider. The output signal of the divider is connected to channel ADC0 of analog-to-digital converter. The signal from the ADC is sent to the FPGA SPI XC3S500E Xilinx Spartan-3E over internal SPI protocol. One of the General Purpose I/O lines (GPIO0) is set to output a pulse position modulation (PPM). two-digit seven-segment LED is used to display the transmitted data.

- Two-channel Scope operates as a standard desktop oscilloscope. The first channel is used to visualize the PPM signal and the second signal is used to display the analog-to-digital convertor's input. [5]

I. PPM Modulator

The Fig. 1 shows the transmitting side of the developed system. The input signal is taken from the Variable Power

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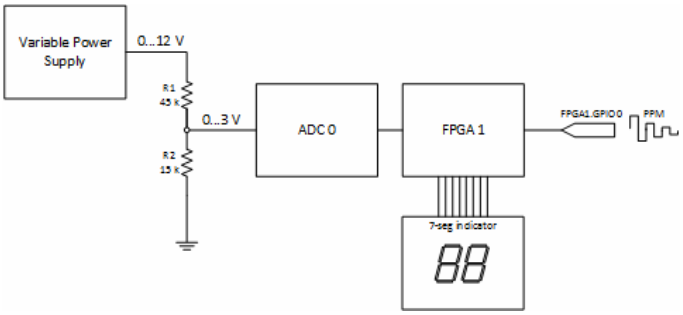

Fig. 1. Block schema of transmission side

The following figure shows the algorithm and interface of the program that implements PPM modulator using NI Digital Electronics FPGA board. It is seen that the algorithm of the program is cyclic, and the interface consists of three indicators. “Processed Value” Scale displays the result after digital processing. “ADC Signal” it is the number that is obtained from the analog-to-digital convertor. "In Range" LED shows if the value obtained from the ADC is in the selected range.

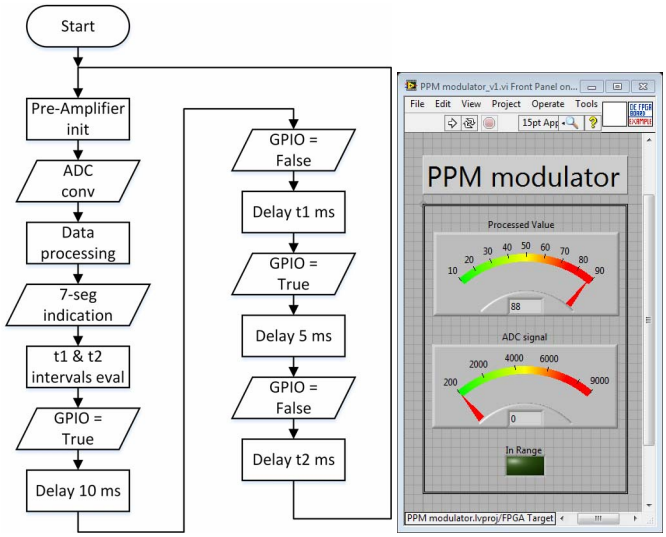

Fig. 2. Algorithm and Interface of the PPM modulator implementation

Both drivers and examples for the board is installed to the personal computer. The installed mock-ups simplify the development of different applications that use NI DE FPGA board. As the basis of this project some example that implements indication of ADC measurements on the soft front panel was carried out. Two virtual instruments from this example was taken: Pre-Amplifier.vi (initialization of pre-amplifier) and AI-read.vi (single ADC measurement). Fig. 3 shows block diagram of PPM modulator.

II. PPM Demodulator

The next Fig. 3 shows a block schema of a receiving side of the system. The input signal is a signal with the pulse position modulation from the transmitting side. Signal enters the GPIO0 line of second FPGA. After demodulation in the chip, the result is indicated on the two-digit seven-segment display.

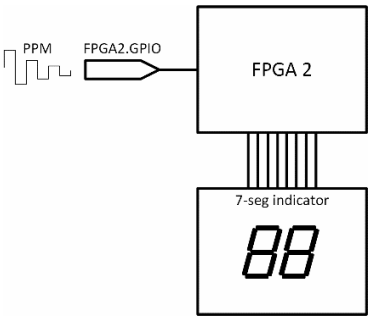

Fig. 3. Block schema of the receiving side

The Fig. 4 shows an algorithm and an interface of PPM demodulator. The algorithm is built on the triggers, allowing to detect leading and trailing edges of pulses at the GPIO0 input. Implementation of a simple high-speed triggers described in details in [6]. When the trigger is activated, the program measures the length of the pulse. The pulse might be a timing or informational. If it is a synchronization pulse the system will wait until the next pulse considering it as informational. Subtracting the start time of an informational pulse from start time of sync pulse the sent data message is got. Then, the received message is displayed on the seven-segment display.

Interface Panel of PPM demodulator.vi has only one indicator that displays the received message.

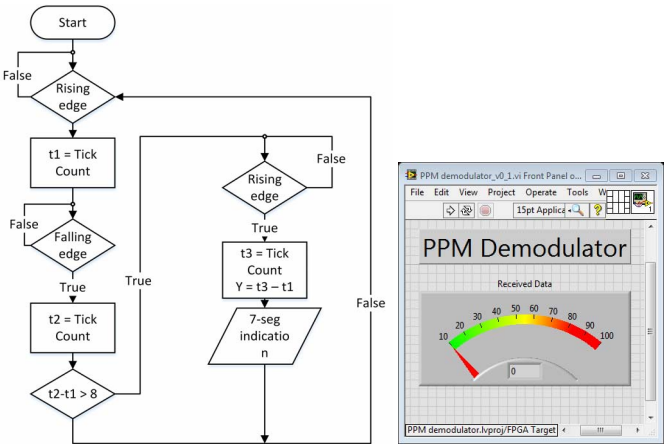

Fig. 4. Algorithm and Interface of the PPM demodulator implementation

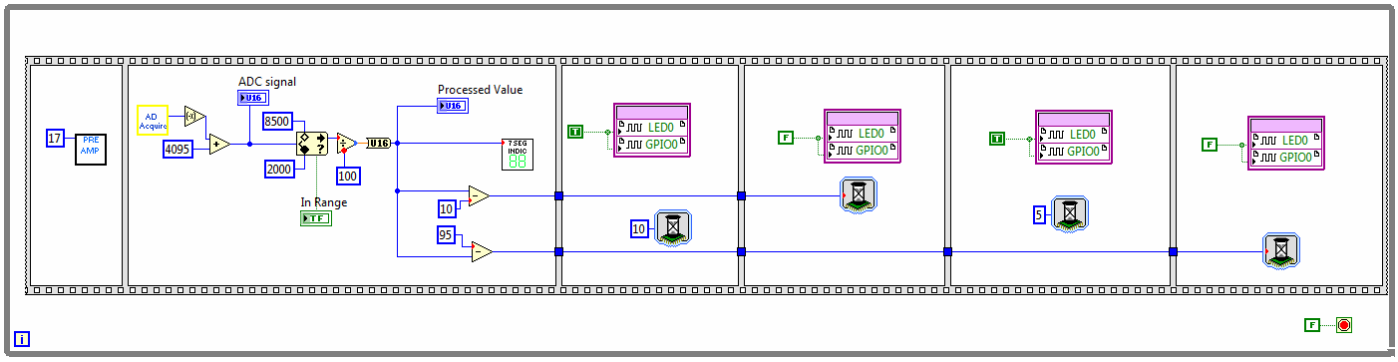

Fig. 5. Block-diagram of PPM modulator.VI

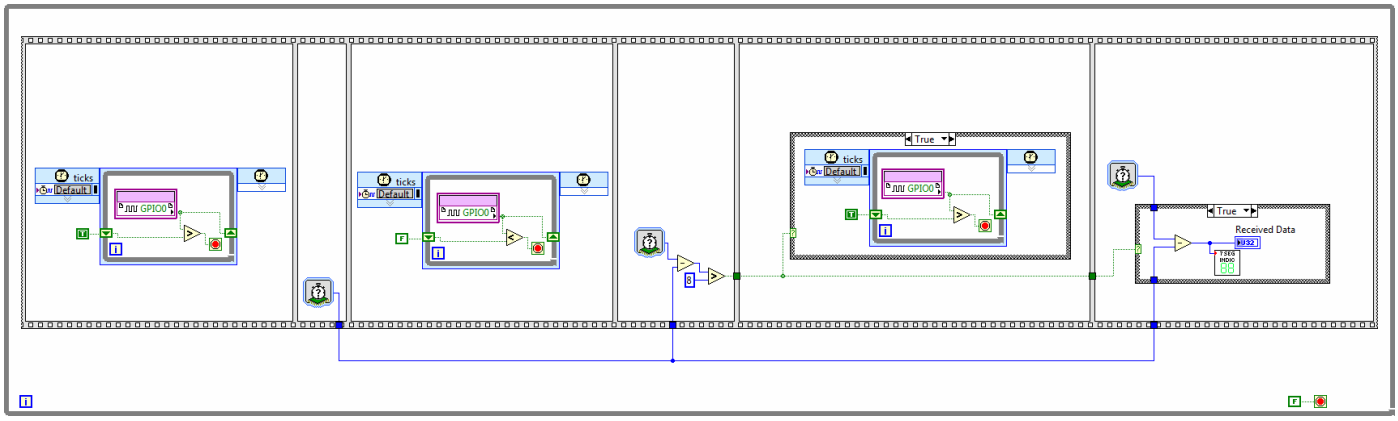

Fig. 6. Block-diagram of PPM demodulator.VI

I. Tests

Designed virtual instruments have been compiled with means of an NI PXI-1075 industrial platform with NI PXIe-8135 embedded controller. Resulted files was uploaded to FPGA Flash-memory of each board.

NI ELVIS II+ laboratory complex simplifies debugging of the project. During the tests ADC is fed by different levels of voltage. GPIO0 channels of both boards were connected by jitter, so we can ignore the noise and attenuation. As a result, errors did not actually observed. Appropriate graphics and photos are shown below in Fig. 5–10.

Oscilloscope settings: vertical scale = 500 mV/div for both channels, horizontal scale 20 ms/div.

The voltage from the Variable Power Supply is sent on a voltage divider. The voltage at the input of the ADC circuit is shown in blue, the output of the modulator in black.

To facilitate the detection of the signal, input is limited in magnitude in the range of 1,3...2,5 V. This is done in order to leave a time space between a synchronizing and information pulses. Time space is 10 ms.

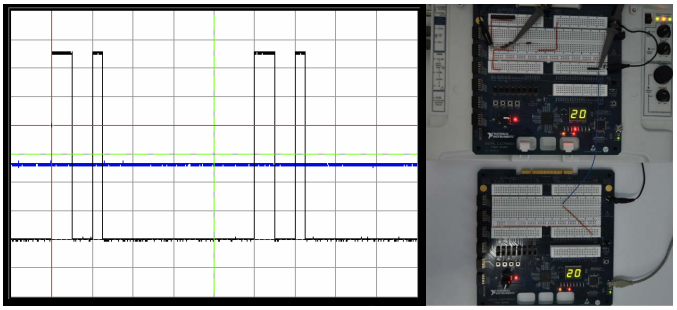

Fig. 7. Test with ADC input in the range 0…1.3 V

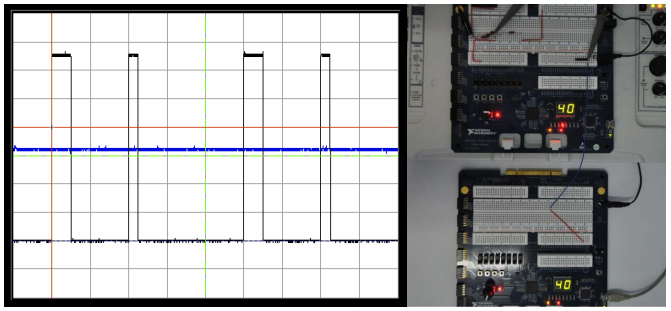

Fig. 8. Test with ADC input 1.6 V

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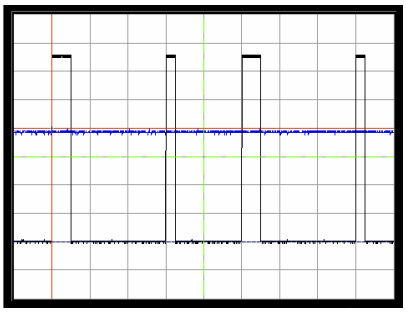

Fig. 9. Test with ADC input 2 V

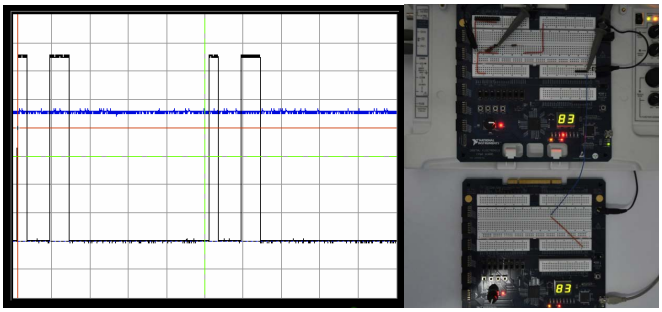

Fig. 10. Test with ADC input 2.25 V

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